128 Mb QSPI

1 GB DDR3

4 GB eMMC *

OSC @ 38.88 MHz

XC7Z015-1CLG485

XC7Z030-15SG485

Processing System

USBI2.0
ULPI PHY

Ethernet
PHY

11 MIO

8 MIO *

JK5 Connector

JK3 Connector

JK2 Connector

Programmable Logic

GTP/GTX

JK5 Micro Header (Bank 13)
20/20 User I/O

JK1 Micro Header (Bank 13)
8/58 User I/O

JK1 Micro Header
50/58 User I/O

JK2 Micro Header (Bank 13)
7/57 User I/O

JK2 Micro Header
50/57 User I/O

JK5 Connector

* eMMC and MIO interfaces shared on JK2.
Zynq 7015/7030 SOC CLG485/SBG485

Embedded eMMC: 2GB, 4GB, 8GB

Jumper A

Boot Mode Select

- eMMC
- 12C/GND
- CPU

Layout Note:
These unused pins shorted intentionally to break out of BGA.

Layout Note:
MGT/MIO0 and MGT/MIO1 signal traces are to be of equal length.
WARNING!!!
Bank 34 and Bank 35 are High
Performance banks (7030 only) and
will only accept 1.8V level signals.
Failure to limit Bank 34 and 35 to
1.8V signals can damage the Zynq
7030 AP SoC.
WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals. Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
Title: 

Size: Rev:

Avnet Engineering Services

Date: 3/11/2016

Document Number: 0

OPTION: DDR3L (1.35V) - R64: 18.7K Ohm

DEFAULT: DDR3 (1.5V) - R64: 15.0K Ohm

Option: DDR3L (1.35V) - R64: 18.7K Ohm

Default: DDR3 (1.5V) - R64: 15.0K Ohm

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### POR_

- S: 1
- P: 2
- G: 3
- R: 4

### FAN

- V: 1
- A: 2
- B: 3

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### Circuit Diagram

- Component labels and connections are detailed in the diagram.
- Please refer to the Avnet Engineering Services Diagram 11 - POWER, RESET.SchDoc for specific component values and connections.

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This diagram provides a comprehensive view of the power and reset functionality, including components such as resistors, capacitors, and voltage regulators.

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Additional notes and specifications are available in the electronic engineering documentation for further reference.
Revision History

Rev B
Original release

Rev C
1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 option note added
5) Renamed 1.5V and DDR3_0V75 power nets
6) Changed U4.2 connection from 1.8V to 3.3V
7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Rev C - Update
1) PUDC Default value changed to VCCO
2) C194 value changed to fix Ethernet Reset RC time constant
3) QSPI_CS resistor value changed to 4.99K

Rev C - Update 3/11/16
1) Updated Block Diagram w/ Both Packages
2) Updated Zynq Symbol Naming w/ Both Packages