Avnet
PicoZed 7015/7030
Revision C
Errata
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1 Introduction

Thank you for your interest in the Avnet PicoZed System-On-Modules. Although Avnet has made every effort to ensure the highest possible quality, these kits and associated software are subject to the limitations described in this errata notification.

Be aware that any of the optional workarounds requiring physical modifications to the board are done at the User’s own risk, and Avnet is not liable for poorly performed rework.

2 Identifying Affected Modules

The modules affected by these errata can be identified by the Revision of the PicoZed System-On-Module. The revision of the PicoZed System-On-Module can be found on the bottom side of the PCB board. The affected PCB boards are the PicoZed 7015 / 7030 Revision C, identified as PCB part number “Z7PZP-Z70xx-PCB-C” and the BOM Revision Part Number, “REVCxx”, where the ‘xx’ is the revision of the BOM on the module.

Figure 1 – Identifying PicoZed 7015/7030 for this Errata

3 Errata

3.1 Ethernet Reset Duration

Applications Affected
Any application that would require the use of PicoZed Ethernet interface.

Description
Resistor/Capacitor circuit R93/C194 of the PicoZed 7015/7030 is affected by this erratum. The resistor/capacitor values that are placed prolongs the Ethernet reset past the 10ms that is required by the PHY. The current time required to release the Ethernet reset is on the order of 30 seconds.

Workaround
If the Ethernet reset duration significantly impacts operation in the end user application a couple of options exist that will allow for proper operation of the Ethernet PHY.

The first option is to do a warm reboot following expiration of the Ethernet reset time. The second option is to modify hardware to change the capacitor value of the resistor/capacitor combo that will allow for a time constant that is closer to the 10ms that is required by the PHY.

Recommended C194 capacitor value: 0.1uF (1206 package)

PicoZed modules supporting the above workarounds are available with boards labelled BD-Z7PZP-Z7015-G REV C03 or BD-Z7PZP-Z7030-G REV C03.
3.2 QSPI Chip Select Current Limiting

Applications Affected
None - There have been not been any adverse functionality reports regarding the on-board QSPI.

Description
1) In Xilinx’s DS187 data sheet the Zynq PS MIO standard current rating is +/- 8mA with a maximum of 10 mA.
   a. The 240 ohm pull-up resistor is an unnecessarily low value. 240 ohms yields an approximate pin current of 12.9mA, which includes the Rds_on value of the PS MIO pin. This exceeds the recommendations provided by Xilinx.
   b. Increasing the resistance from 240 ohms to 4.99K ohms reduces the pin current to approximately 0.661mA while ensuring QSPI_CS signal is pulled low enough to be valid for the QSPI device.

Workaround
The QSPI Chip Select pull-up resistor value has been increased from 240 ohms to 4.99K ohms. On PicoZed 7015/7030, the QSPI Chip select is reference designator R75.

PicoZed 7015/7030 modules supporting the above workaround are available with boards labelled BD-Z7PZP-Z7015-G REV C03 or BD-Z7PZP-Z7030-G REV C03.

3.3 No 12V VIN Support

Applications Affected
Any application that would require the use greater than 5V DC and less than 12V DC as the input from a Carrier Card to the PicoZed 7015/7030 System-On-Modules.

Description
The 1.0V power supply, U11 on the PicoZed 7015/7030 is affected by this erratum. The VIN input voltage to the TPS54618 power supply is restricted to 5V VIN only.

The input voltage to the PicoZed 7015/7030 board are provided via the VIN pins on the JX1/JX2/JX3 connectors on the System-On-Modules. An end user Carrier Board should be designed to provide 5V DC on the VIN pins of the System-On-Module due to the 1.0V power supply.

3.4 PUDC Default Setting

Applications Affected
Any application that would require PUDC set to GND by default.

Description
In order to support uniformity in the MicroZed and PicoZed product families, the default setting for the PUDC (Pull-Up during Configuration) pin on the Zynq device should be consistent. The PicoZed 7015/7030 inadvertently set the default state to GND when the MicroZed and PicoZed 7010/7020 sets the default state to VCCO.

Workaround
Move the 1K 0402 resistor on JT2 to the position covering Pin 2 to Pin 3 to set the PUDC to VCCO.

PicoZed modules supporting the above workarounds are available with boards labelled BD-Z7PZP-Z7015-G REV C03 or BD-Z7PZP-Z7030-G REV C03.
3.5 TPS54618 EN Voltage Threshold

Applications Affected
All 7015 and 7030 PicoZed modules, Revision C03 or earlier.

Description
The PicoZed 7015 and 7030 modules use the Texas Instruments TPS54618 for core power. There is an error in the design where the ENABLE pin on this device is pulled up to Vin (5V) through a 10k resistor (R52). The maximum voltage on this pin is 4V. Exposing this pin to 5V may result in device damage where the EN pin develops a short to ground.

This pin has an internal pullup, therefore the external pull-up is unnecessary. The TPS54618 EN pin is connected to the PWR_ENABLE signal on PicoZed, which is connected to JX1.pin5. The Avnet PicoZed FMC Carrier Card original as well as PicoZed FMC Carrier Card V2 both will drive this pin low when power is off or let it float when power is on.

Workaround
Remove R52, which is the pullup resistor, on all 7015 and 7030 modules.

Figure 2 – Remove R52 on PicoZed 7015/7030 Rev C03 and Earlier

PicoZed modules with the above workaround implemented are labelled BD-Z7PZP-Z7015-G REV C04 or BD-Z7PZP-Z7030-G REV C04.
3.6 VCCO_34/35 Limitation between 7010/20 and 7015/30

Applications Affected
Designs that would like to migrate between PicoZed 7010/20 modules and PicoZed 7015/30 modules.

Description
When the PicoZed 7015/30 PCB was designed, it made more sense to rotate the Zynq device 180 degrees in comparison to the 7010/20 PCB. This allowed for easier transceiver routing from the 7015/30 Zynq device to JX3. With the rotation, it also made more sense to put the Bank 35 I/Os on JX1 and the Bank 34 I/Os on JX2.

Although the Bank 34 and 35 I/Os were exchanged on JX1/JX2, the VCCO pins were not. This leads to a limitation if you plan to design a carrier that supports multiple members of the PicoZed family:

If the Carrier has different voltages on VCCO_34 and VCCO_35, then the Carrier cannot migrate between the 7010/20 and 7015/30. Only one family pair can be supported.

Avnet's PicoZed FMC Carrier Card original and PicoZed FMC Carrier Card V2 shares the same voltage on VCCO_34 and VCCO_35, therefore, it can support any of the PicoZed SOMs.

If you only plan to migrate between the 7010 and 7020 or the 7015 and 7030, then you will also not have this limitation.

Workaround
Here are some suggestions for a PicoZed Carrier Design that could support different voltages on VCCO_34 and VCCO_35 as well as PicoZed migration:

- Consider using jumper options to custom configure each bank supply based on the populated module
- Consider using a programmable voltage supply, such as a PMBus-enabled device, that can be adjusted based the populated module.
### 3.7 eMMC Read Errors at Startup and Cold Temperatures When Using High-Speed Mode

#### Applications Affected

All PicoZed SOM designs that access the eMMC in the default high-speed mode at startup or in a cold environment may experience readback failures. For example, using the eMMC as the secondary boot source for booting Linux may encounter a readback error when U-boot attempts to read back the image.ub from the eMMC. Approximately 25% of all PicoZed SOMs are affected. This affects all four densities of PicoZed and both temperature grades, including kits that use these SOMs. The affected part numbers are:

- AES-Z7PZ-7Z010-SOM-G
- AES-Z7PZ-7Z015-SOM-G
- AES-Z7PZ-7Z020-SOM-G
- AES-Z7PZ-7Z030-SOM-G
- AES-Z7PZ-7Z010-SOM-I-G
- AES-Z7PZ-7Z015-SOM-I-G
- AES-Z7PZ-7Z020-SOM-I-G
- AES-Z7PZ-7Z030-SOM-I-G
- AES-Z7PZ-SVDK-G

This issue is discussed in forum topic [http://picozed.org/content/picozed-fails-load-os-emmc-low-temp](http://picozed.org/content/picozed-fails-load-os-emmc-low-temp).

#### Description

By default, several Xilinx applications place the SDIO controller in High-speed Mode (HSM). This mode is described in *Embedded MultiMediaCard(eMMC) eMMC/Card Product Standard, (MMCA, 4.41)*. The alternative is referred to by Xilinx as Standard-speed Mode (SSM), while the MMCA 4.41 refers to this as *Backward-compatible card interface timing*. The timing parameters for both these modes are described in MMCA 4.41 *Figure 64 — Timing diagram: data input/output* as well as *Table 113 — High-speed card interface timing* and *Table 114 — Backward-compatible card interface timing*.

In both modes, the input data is sampled on the rising edge. The difference is the mechanism for outputting data. In SSM, the data is output on the falling edge of the SDIO clock, while in HSM, the data is output on the rising edge of the clock.

Xilinx provides some information about these modes in Answer Record 59999 at [http://www.xilinx.com/support/answers/59999.html](http://www.xilinx.com/support/answers/59999.html). This Answer Record provides a design advisory that acknowledges that the Zynq-7000 is not fully compliant with the MMC JEDEC standard 4.41 in that the minimum hold time may be violated. Although the modes described in this document are relevant to the PicoZed issue, the specific issue is not. Avnet has received NDA information from Micron that shows the Micron eMMC used on PicoZed has characterization data showing < 2.0 ns hold time that is required by the Zynq-7000.

The primary failure mode that was discovered in the field was a PetaLinux boot failure during U-boot. Examples of failure messages detected include:

```
sdhci_transfer_data: Error detected in status(0x208000)!
Error reading cluster
** Unable to read file image.ub **
U-Boot-PetaLinux>
```

Or

```
** Unrecognized filesystem type **
U-Boot-PetaLinux>
```

After extensive testing, it was shown that these failures could be eliminated by using SSM at a maximum rate of 25 MHz rather than HSM, which is the default for both U-boot and PetaLinux.
**Workaround**
PicoZed eMMC must be operated in SDIO SSM at a rate of 25 MHz or less. SSM must be used in both U-boot and PetaLinux. This does not affect the data width; therefore, a data width up to 4 bits is supported.

An example for U-boot and PetaLinux SSM is provided in the updated 2016.2 PetaLinux BSPs that are posted at on the PicoZed Carrier pages:

http://picozed.org/support/design/13076/106

http://picozed.org/support/design/4701/76

**PetaLinux Board Support Packages**
Compressed PetaLinux BSPs for Avnet Zynq system platforms.

PetaLinux 2016.2 Compressed BSP, z7010

PetaLinux 2016.2 Compressed BSP, z7015

PetaLinux 2016.2 Compressed BSP, z7020

PetaLinux 2016.2 Compressed BSP, z7030

Figure 3 – View on picozed.org
3.8 Industrial PicoZed 7030 Rev C04 Build Mistake Affecting Ethernet Reset

Applications Affected
One build of PicoZed 7030 Industrial SOMs, Revision C04 were built with two incorrect component values. This issue is discussed in forum topic [http://picozed.org/content/pz-7030i-build-issue-affects-ethernet-reset](http://picozed.org/content/pz-7030i-build-issue-affects-ethernet-reset).

Description
Our CM mistakenly populated two component sites with values from earlier revision BOMs. The affected boards are:

- Revision C04
- P/N BD-Z7PZP-7Z030I-G
- Unit Serial are: from 1428858 to 1429007

![Figure 4 – Example of Failing PicoZed 7030 Industrial Serial Number](image)

One component affected is C194, which is populated as 100uF when it should be 0.1uF. This has the undesired effect of delaying the Ethernet Reset for ~30 seconds, after which the Ethernet operates correctly. This is the problem identified in Erratum 3.1. This problem was corrected on Rev C03, and it is correct on other C04 boards.

The other component affected is R75, which is populated as 240 ohms when it should be 4.99K-ohm. This does not affect the functionality of the board. This problem was previously identified in Erratum 3.2. This was also corrected on Rev C03 and is correct on other C04 boards.

Workaround
If you have received boards in this serial number range, please contact your Avnet representative. Avnet will either repair returned boards or send correct components if it is easier for you to replace these two components locally.
3.9 Extra USB 2.0 Capacitors on SOM

**Applications Affected**
Currently, there are no known field failures due to this issue. However, it could potentially affect any PicoZed application utilizing the USB 2.0 interface. The affected part numbers are:

- AES-Z7PZ-7Z010-SOM-G
- AES-Z7PZ-7Z015-SOM-G
- AES-Z7PZ-7Z020-SOM-G
- AES-Z7PZ-7Z030-SOM-G
- AES-Z7PZ-7Z010-SOM-I-G
- AES-Z7PZ-7Z015-SOM-I-G
- AES-Z7PZ-7Z020-SOM-I-G
- AES-Z7PZ-7Z030-SOM-I-G
- AES-Z7PZ-SVDK-G

**Description**
The Microchip USB3320 outlines very specific capacitance guidelines for setting the PHY mode to Host, Device, or OTG. To keep the PicoZed as flexible as possible, the Mode setting capacitors must be placed on the Carrier based on the operating USB mode the user requires. On Rev C, extra bypass capacitors were placed on the JX3 connector that may interfere with this mode setting.

![Figure 5 – Extra Caps on PicoZed 7015/30 Rev C](image)

**Workaround**
Depopulate C190, C191, and C192 on the SOM.

This fix is implemented on PicoZed 7015/7030 Revision D.
4 New Erratum

Any new erratum found will be posted to the PicoZed website: www.picozed.org

5 Additional Support

For additional support, please review the discussions and post your questions to the PicoZed Forums at http://picozed.org/forums/picozed-hardware-design

You can also contact your local Avnet FAE.
## 6 Revision History

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<td>Initial Version, PicoZed 7015/7030 Rev C</td>
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<tr>
<td>17 Jul 2015</td>
<td>1.1</td>
<td>Corrected BOM Version</td>
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<tr>
<td>10 May 2016</td>
<td>1.2</td>
<td>Addition of sections 3.5 and 3.6</td>
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<td>15 Nov 2016</td>
<td>1.3</td>
<td>Addition of sections 3.7 and 3.8</td>
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<td>22 Aug 2017</td>
<td>1.4</td>
<td>Added Item 3.9, Extra USB 2.0 Capacitors on SOM</td>
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