UltraZed-EV Carrier Card

Revision: 1

UltraZed-EV Carrier Card
Avnet Engineering Services
www.avnetkits.com

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Note:
ULTRAZED EV CARRIER CARD BLOCK DIAGRAM
uSD, MAC, GIGE, SATA I/F

**Micro SD Card**

**SATA Interface**

**SOM Gb ETH 10/100/1000**

**MAC ID - EEPROM**

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**Layout Note:**

- Insert a 20-25Ω via between CMD, data and SD, CLC. Place SDCLK resistor within 25m of J connector.
- Insert a 100 mil resistor within 100 mils of JX connector.

**Resistor:**

- 4.99K
- 100 mils of JX connector.

**Components:**

- R38
- C54
- 0.1uF
- 1.00K
- 0.01uF
- 240R
3G-SDI INTERFACE (SMPTE) & PCIe ROOT PORT

Layout Note: GTH Z_SE = 75 Ohms (to ground).

JP3 Open = Enable (default) JP4 Open = HD/3G Operation (default)
JP5 Open = HD/3G Operation (default) JP6 Open = HD/3G Operation

PCIe Root Port x1

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SCH-US3CAR

2/5/2018
Legend Note: SFP+ 2x40G Chrev Diff

SFP+ INTERFACE 1

OPERATIONAL NOTE:
JP9: PLACED = Optical TX Enabled
JP9: NOT PLACED = Optical TX Disabled
Default: JP9=PLACED

SFP+ INTERFACE 2

OPERATIONAL NOTE:
JP9: PLACED = Optical TX Enabled
JP9: NOT PLACED = Optical TX Disabled
Default: JP9=PLACED

UltraZed-EV Carrier Card
JX1 CONNECTOR
JX2 CONNECTOR & PL PMODS

Layout Notes:
1. No pin swapping allowed.
2. Differential pairs: Route at 100 Ohms unless otherwise noted.

LOOBACKS

JX2 JB PL PMOD

Legend Note:
ALL PMODs routed single ended at 50 ohms.
LED INDICATORS

PS USER LED

POWER SUPPLY LEDS

1.2V
0.85V
0.9V
1.8V
1.8V
3.3V_BANKS
3.3V_MAIN
3.3V_PRI
User's Note: TXD and RXD are swizzled on this interface to create null modem connections.

Layout Note: USB DP & DN signals routed 90 ohm differentially, 45 ohm single ended.
POWER INPUT
NOT ATX COMPATIBLE
120W+ POWER ONLY

NOTE: NEW PINOUT FOR 120W+ PSU

1.8V MAIN (HIGH CURRENT)
For Bode plot testing

D2C Address Offset = +11. Addresses: 0x1B, 0x0B.

3.3V MAIN (HIGH CURRENT)
For Bode plot testing

D2C Address Offset = +12. Addresses: 0x1C, 0x0C.

FAN HEADER

+1.8V NET TIES
+3.3V NET TIES

POWER 1

+PS_VBATT_TEST

VOLTAGE MONITOR HEADERS

SYSMON HEADER

PMBus HEADER

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POWER 3

IC Address Offset = +10. Addresses: 0x1A, 0x4A.

NOTE: MTP resistor set to allow 0x9 address skip.