UltraZed IO Carrier Card

Revision: 1
CLOCK SYNTHESIZER & LVDS PORT

IDT CLOCK SYNTHESIZER

Layout Note: Differential pairs: Route at 100 ohms. Termination on JX3 connectors.

CLOCK SYNTHESIZER

LVDS CONNECTOR

Layout Note: Differential pairs: Route at 100 ohms. Termination on JX3 connectors.

User Note: SEL [0/1]: Mode [default]

I2C Mode: JP1 not installed, J1/J2 installed.
Layout Note: Arduino JA1 are the DCC notch names, not the port connector names. These are single ended. See FSG.

User's Note: The analog interface is an output only from the Arduino shield.
JX2 HP PL PMODs

- JX2 JA PL PMOD
- JX2 JB PL PMOD
- JX2 JC PL PMOD
- JX2 JD PL PMOD
- JX2 JE PL PMOD
- JX2 JF PL PMOD

Note: All PMODs routed single ended at SC board.

Avnet Engineering Services

Size:

BOM:
User’s Note: TXD and RXD are swizzled on this interface to create null modem connections.