Embedded eMMC: 4GB, 8GB (default), 16GB, 32GB, 64GB

This eMMC footprint is based on the 169-ball WFBGA 14.0mm x 12.5mm package. This footprint is compatible with the 155-ball WFBGA 13.5mm package if space is populated. See the Hardware User Guide for a conversion table.

Boot Mode Select
Revisions:

**Revision B1:**
1. Multiplexed JX2 MIO signals with EMMC
2. Removed Push Button Footprint
3. Incorporated ETHERNET RESET circuit
4. Added bulk cap to AVDD18
5. Added GND Testpoints

**Revision B2:**
1. Updated BOOT MODE table
2. Added shared circuit MIO47 to JX3 and ETHERNET RESET
3. Added RC time constant to ETHERNET RESET
4. Changed DDR3L / DDR3 Option Added
5. Added bulk cap to AVDD18
6. Added GND Testpoints

**Revision C:**
1. Updated Block Diagram
2. Added shared circuit MIO47 to JX3 and ETHERNET RESET
3. Added RC time constant to ETHERNET RESET
4. DDR3L / DDR3 Option Added
5. Modified resistor divider value on PG_1V8
6. Changed DDR3 Termination Regulator VLDOIN from 1.8V to 3.3V

**Revision C (Errata):**
1. R71: Changed to 4.99K
2. R182: Changed to 0.1uF

**Revision D:**
1. U1, U2, JT1, JT2, and JT6 have been removed
2. U3, U6, and U15 part numbers changed
3. Moved U12, R15, C12, C19, and C20 away from FPGA to allow for heatsink clearance
4. JTs and JF9 added to allow Boot Mode to be hard wired with 0 Ohm Jumpers
5. JTs Replaced with 4.99K Pulldown resistor

**Revision E:**
1. Connected U6 Pin B3 to GND
2. Added Voltage Divider (R84, R95) and filter cap (C62) to U15 "VRI" pin
3. Added C133 and C184 to U15 Pin 3/5 (DDR3_VTT)
4. Added C63 to U15 Pin 2 (PVcc)
5. Changed C47 to 0.1uF Cap
6. Changed C171 to 4.7uF Cap