

# Network FMC User Guide

Version 1.0

# Document Control

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# 1 Network FMC Overview

This document provides the functional and technical design information for the Network FMC board. The objectives of the board are listed below:

- This FMC networking personality module supports 10/100/1000 Mb/s
- Allows for expanded I/O operating voltage range from 1.8V to 3.3V modes
- Implements two PHYs with RGMII capabilities
- All components support industrial operating temperature of -40C to +85C

## 2 Block Diagram and Features

This section summarizes the features of the board, followed by further detailed information.

### 2.1 List of Features

The Network FMC Board supports the following features:

- 10/100/1000 Mb/s RGMII PHY x 2
- Ethernet MAC ID EEPROM (32 Kb) x 2
- FMC IPMI SEEPROM (2 Kb)
- FMC LPC Connector
- Board LEDs
- Ethernet PHY Clock Source – 25Mhz x 2
- Ethernet MAC Clock Source 125MHz
- PWM Controller 1.2V Regulator

## 2.2 Block Diagram

Below is a high level block diagram of the Network FMC Board.

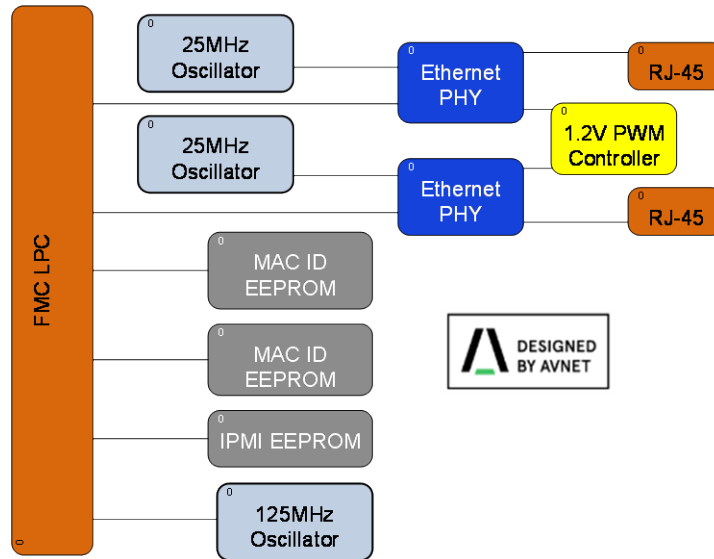


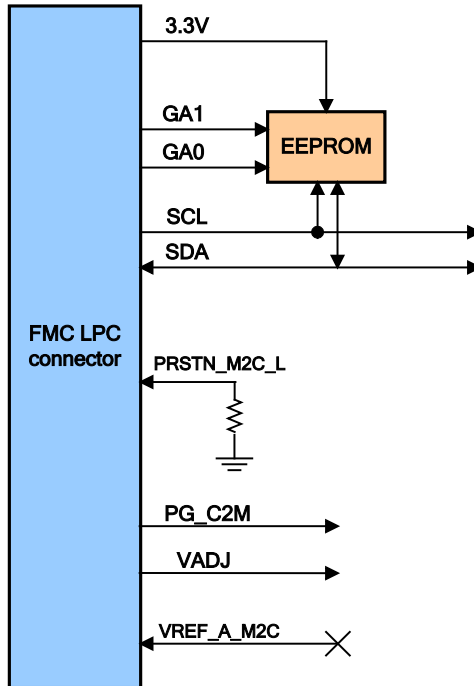
Figure 1 – Network FMC – High Level Block Diagram

## 3 Functional Description

The following section details the features of the Network FMC board.

### 3.1 IPMI Identification I2C EEPROM

The Intelligent Platform Management Interface (IPMI) EEPROM utilizes an Atmel AT24C02D. This EEPROM provides module characterization information to the carrier board for proper voltage settings. The carrier detects the presence of an FMC module by verifying that PRSTN\_M2C\_L is asserted low. It then queries the I2C EEPROM to discover which voltage is requested by the module for VADJ. The requirement and protocol are detailed in the VITA-57 specification.



**Figure 2 – IPMI Identification – Block Diagram**

Before the module is powered-up, the carrier must identify the FMC module. At this point, the main power to the module is off. Only the auxiliary 3.3V power rail (3P3VAUX) is active.

The carrier detects the presence of an FMC module by verifying that PRSTN\_M2C\_L is asserted low. It then queries the I2C EEPROM to discover which voltage is requested by the module for VADJ. The EEPROM for this module will support 1.8V. All other voltages must be manually asserted.

The carrier will power up the module by applying the requested voltage to VADJ. When the voltage is valid, the PG\_C2M (ie. power good) will be asserted high. This will be visible via LED D6. A inverted version of this signal is used to enable all the voltage level translators connected to VADJ.

The address of the IPMI I2C EEPROM will be determined by the GA[0:1] signals driven by the carrier.

Table 1 describes the normal EEPROM address, and the actual EEPROM address for the Network FMC module.

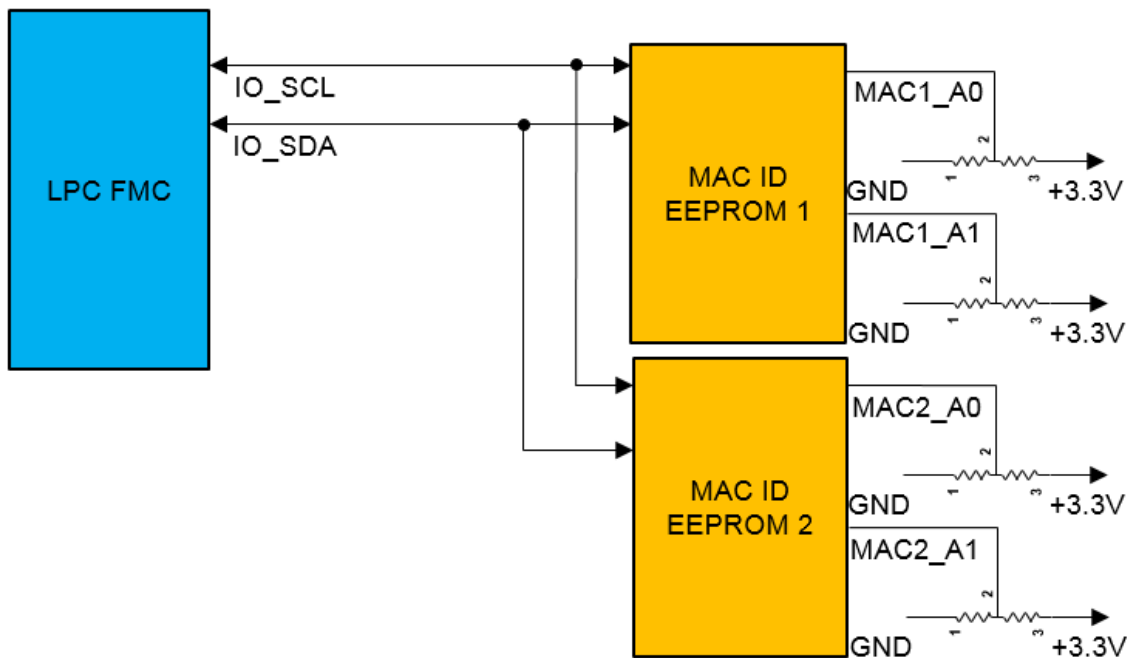
Network FMC	
GA[0:1]	I2C IPMI EEPROM Address
00	0xA0
01	0xA2
10	0xA4
11	0xA6

**Table 1 – IPMI Identification – I2C EEPROM Address**

There will be three separate I2C lines, one dedicated for each EEPROM present on the FMC Module. The three EEPROMS consist of two Microchip 24AA025-E48-I/SN MAC EEPROMs and the one Atmel AT24C02D IPMI EEPROM. Each I2C line will have the option to be tied together into a single I2C line by populating the 0 Ohm resistors at R94, R95, R115, R116, and removing the 0 Ohm resistors at R111, R112, R113, and R114.

### 3.2 I2C MAC EEPROM Configuration – E48 Compliant

The two E48 compliant I2C MAC EEPROM configurations provide a unique MAC address which are used for each of the on-board PHYs. The two EEPROMs are made up of two Microchip 24AA025-E48-I/SN components. Configuration resistors are used to achieve the correct address.



**Figure 3 – I2C MAC EEPROM Configuration – Block Diagram**



The following table lists the I2C addresses that are present on each of the I2C Multiplexer's ports by default. Notice that the I2C Multiplexer's address is always visible regardless of which port is enabled.

Device	I2C Address
MAC ID EEPROM 1	0xA0 (24AA025E48)
MAC ID EEPROM 2	0xA0 (24AA025E48)

**Table 2 – I2C Peripheral Configuration – Device Summary**

There will be three separate I2C lines, one dedicated for each EEPROM present on the FMC Module. The three EEPROMS consist of two Microchip 24AA025-E48-I/SN MAC EEPROMs and the one Atmel AT24C02D IPMI EEPROM. Each I2C line will have the option to be tied together into a single I2C line by populating the 0 Ohm resistors at R94, R95, R115, R116, and removing the 0 Ohm resistors at R111, R112, R113, and R114.

### 3.3 Microchip 10/100/1000 Mb/s RGMII PHY x 2

Two 10/100/1000 Mb/s Microchip KSZ9031RNXI RGMII PHYs are used on the Network FMC board. The datasheet can be found at <http://www.Microchip.com/wwwproducts/en/KSZ9031>

The Microchip KSZ9031RNXI RGMII PHY has many strapping configurations as per your desired configurations. Each Microchip PHY has the same default strapping configurations on the Network FMC board. Resistor jumpers are provided for each PHY strapping configuration. Please view the schematic to determine what resistor jumpers must be removed and added to obtain desired configuration if different from the default configuration is desired. See Table 3 below.

KSZ9031RNXI Pin Number	Pin Name	Type	Default Configuration	Description																																		
35	PHYAD2	I/O	Pull-Down	The PHY address, PHYAD[2:0], is sampled and latched at power-up/ reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows: Pull-up = 1 Pull-down = 0 PHY Address Bits [4:3] are always set to '00'.																																		
15	PHYAD1	I/O	Pull-Down																																			
17	PHYAD0	I/O	Pull-Up																																			
27	MODE3	I/O	Pull-Up	<table border="1"> <thead> <tr> <th>MODE[3:0]</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>Reserved - not used</td> </tr> <tr> <td>0001</td> <td>Reserved - not used</td> </tr> <tr> <td>0010</td> <td>Reserved - not used</td> </tr> <tr> <td>0011</td> <td>Reserved - not used</td> </tr> <tr> <td>0100</td> <td>NAND tree mode</td> </tr> <tr> <td>0101</td> <td>Reserved - not used</td> </tr> <tr> <td>0110</td> <td>Reserved - not used</td> </tr> <tr> <td>0111</td> <td>Chip power-down mode</td> </tr> <tr> <td>1000</td> <td>Reserved - not used</td> </tr> <tr> <td>1001</td> <td>Reserved - not used</td> </tr> <tr> <td>1010</td> <td>Reserved - not used</td> </tr> <tr> <td>1011</td> <td>Reserved - not used</td> </tr> <tr> <td>1100</td> <td>RGMI mode - Advertise 1000BASE-T full-duplex only</td> </tr> <tr> <td>1101</td> <td>RGMI mode - Advertise 1000BASE-T full- and halfduplex only</td> </tr> <tr> <td>1110</td> <td>RGMI mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex), except 1000BASE-T halfduplex</td> </tr> <tr> <td>1111</td> <td>RGMI mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex)</td> </tr> </tbody> </table>	MODE[3:0]	Mode	0000	Reserved - not used	0001	Reserved - not used	0010	Reserved - not used	0011	Reserved - not used	0100	NAND tree mode	0101	Reserved - not used	0110	Reserved - not used	0111	Chip power-down mode	1000	Reserved - not used	1001	Reserved - not used	1010	Reserved - not used	1011	Reserved - not used	1100	RGMI mode - Advertise 1000BASE-T full-duplex only	1101	RGMI mode - Advertise 1000BASE-T full- and halfduplex only	1110	RGMI mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex), except 1000BASE-T halfduplex	1111	RGMI mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex)
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28	MODE2	I/O	Pull-Up																																			
31	MODE1	I/O	Pull-Up																																			
32	MODE0	I/O	Pull-Up																																			

33	CLK125_EN	I/O	Pull-Down	CLK125_EN is sampled and latched at power-up/reset and is defined as follows: Pull-up (1) = Enable 125 MHz clock output Pull-down (0) = Disable 125 MHz clock output Pin 41 (CLK125_NDO) provides the 125 MHz reference clock output option for use by the MAC.
41	LED_MODE	I/O	Pull-Up	LED_MODE is sampled and latched at power-up/reset and is defined as follows: Pull-up (1) = Single-LED mode Pull-down (0) = Tri-color dual-LED mode

**Table 3 – Ethernet PHYs Strapping Configurations**

### 3.4 RJ45 Connectors

The two Bel Fuse L829-1J1T-32 Ethernet RJ45 connectors contain integrated magnetics. The RJ45 connectors also have integrated LEDs, one yellow single color led, and one green orange bi-color led. In the default configuration the PHYs are setup in single-LED mode, so only the yellow single color led and the green in the bi-color led are being used by default. However, strapping resistors are provided to change both the PHYs to operate in tri-color dual-LED mode and to enable the orange bi-color led. Please refer to the schematic to determine these resistors.

### 3.5 Power

A Microchip MIC23050-4YML-TR PWM Buck Regulator is used to drop the 3.3V in from FMC header to 1.2V to be used by the two Ethernet PHYs. This buck regulator has an output current of 600mA.

It is very important that the 1.2V core rail powered by the MIC23050-4YML-TR comes up either 200us before the 3.3V and 1.8V power rails, or within 1ms after the 3.3V and 1.8V power rails stabilize. To ensure this a RC time constant delay circuit was placed on the enable pin of the MIC23050-4YML-TR regulator. In stressed industrial applications a Schmitt trigger should be placed.

All other voltage sources are supplied from the LPC FMC connector. The following table lists all the voltage sources involved in the Network FMC Solution.

Voltage Name	Voltage	Description
<b>Supplied by FMC Connector</b>		
3.3VAUX	3.3 V	Used by IPMI Identification prior to module power-up.
3.3V	3.3 V	Used by onboard 25MHz clock, 125MHz clock, and driver
VADJ	1.8 V or 2.5 V or 3.3 V	Used for all single-ended signals connected to FMC connector.
12V	12.0 V	Not Used
<b>Not Supplied by FMC Connector</b>		
1.2V	1.2V	Supplied by MIC23050-4YML-TR for PHY

**Table 4 – Network FMC - Voltage Sources**

**3.6 FMC LPC Connector:**

An FMC Low Pin Count connector will be used to provide all interface aspects (data, power, clocks, reset, etc.) to this board. This connector format also enables compatibility with all Xilinx FPGA and SoC development boards.

The FMC LPC connector is defined as follows:

	H	G	D	C
1	VREF A M2C	GND	PG C2M	GND
2	PRSNT M2C L	CLK1 M2C P	GND	DP0 C2M P
3	GND	CLK1 M2C N	GND	DP0 C2M N
4	CLK0 M2C P	GND	GBTCLK0 M2C P	GND
5	CLK0 M2C_N	GND	GBTCLK0 M2C_N	GND
6	GND	LA00 P CC	GND	DP0 M2C P
7	LA02 P	LA00 N CC	GND	DP0 M2C N
8	LA02 N	GND	LA01 P CC	GND
9	GND	LA03 P	LA01 N CC	GND
10	LA04 P	LA03 N	GND	LA06 P
11	LA04 N	GND	LA05 P	LA06 N
12	GND	LA08 P	LA05 N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12 P	LA09 N	LA10 N
16	LA11 P	LA12 N	GND	GND
17	LA11 N	GND	LA13 P	GND
18	GND	LA16 P	LA13 N	LA14 P
19	LA15_P	LA16_N	GND	LA14 N
20	LA15 N	GND	LA17 P CC	GND
21	GND	LA20 P	LA17 N CC	GND
22	LA19 P	LA20 N	GND	LA18 P CC
23	LA19 N	GND	LA23 P	LA18 N CC
24	GND	LA22 P	LA23 N	GND
25	LA21 P	LA22 N	GND	GND
26	LA21 N	GND	LA26 P	LA27 P
27	GND	LA25 P	LA26 N	LA27 N
28	LA24 P	LA25 N	GND	GND
29	LA24 N	GND	TCK	GND
30	GND	LA29 P	TDI	SCL
31	LA28 P	LA29 N	TDO	SDA
32	LA28 N	GND	3P3VAUX	GND
33	GND	LA31 P	TMS	GND
34	LA30 P	LA31 N	TRST L	GA0
35	LA30 N	GND	GA1	12P0V
36	GND	LA33 P	3P3V	GND
37	LA32 P	LA33 N	GND	12P0V
38	LA32 N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND

LPC Connector      LPC Connector      LPC Connector      LPC Connector

**Table 5 – FMC LPC Connector Pinout**

**Note:** For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

The FMC LPC pin allocation for the Network FMC module is defined in Table 6.

	H	G		D	C	
1	-	GND	1	PG_C2M	GND	1
2	PRSNT_M2C_L	-	2	GND	-	2
3	GND	-	3	GND	-	3
4	M2C_125MHZ_P	GND	4	-	GND	4
5	M2C_125MHZ_N	GND	5	-	GND	5
6	GND	ETH1_RX_CLK	6	GND	-	6
7	ETH1_RX_D0	ETH1_RX_EN	7	GND	-	7
8	ETH1_RX_D1	GND	8	ETH2_RX_CLK	GND	8
9	GND	ETH1_RX_D2	9	ETH2_RX_EN	GND	9
10	ETH1_TX_D0	ETH1_RX_D3	10	GND	ETH2_RX_D0	10
11	ETH1_TX_CLK	GND	11	ETH1_MDC	ETH1_MDIO	11
12	GND	ETH1_TX_D1	12	ETH1_RST_N	GND	12
13	ETH1_TX_D3	ETH1_TX_D2	13	GND	GND	13
14	ETH1_TX_EN	GND	14	ETH2_RX_D1	-	14
15	GND	-	15	ETH2_RX_D3	ETH2_RX_D2	15
16	ETH2_TX_D1	ETH2_TX_D0	16	GND	GND	16
17	ETH2_TX_CLK	GND	17	M2C_125MHZ_EN	GND	17
18	GND	ETH2_TX_D2	18	ETH2_MDC	M2C_125MHZ_SEL	18
19	ETH2_TX_EN	ETH2_TX_D3	19	GND	ETH2_MDIO	19
20	ETH2_RST_N	GND	20	-	GND	20
21	GND	-	21	-	GND	21
22	-	-	22	GND	-	22
23	-	GND	23	-	-	23
24	GND	-	24	-	GND	24
25	-	-	25	GND	GND	25
26	-	GND	26	LED2A	LED1A	26
27	GND	LED3A	27	LED2B	LED1B	27
28	LED4A	LED3B	28	GND	GND	28
29	LED4B	GND	29	-	GND	29
30	GND	-	30	TDI	SCL	30
31	LED5A	-	31	TDO	SDA	31
32	LED5B	GND	32	3P3VAUX	GND	32
33	GND	SCL2	33	-	GND	33
34	-	SDA2	34	-	GA0	34
35	-	GND	35	GA1	12P0V	35
36	GND	-	36	3P3V	GND	36
37	SCL1	-	37	GND	12P0V	37
38	SDA1	GND	38	3P3V	GND	38
39	GND	VADJ	39	GND	3P3V	39
40	VADJ	GND	40	3P3V	GND	40

**Table 6 – Network FMC – FMC Pinout**

### 3.7 Board LEDs

- D1 - Bi-Color Red/Green Led used for Network Status
- D2 - Bi-Color Red/Green Led used for Module Status
- D3 - Bi-Color Green/Yellow Led used for User Led 1/Link/Activity
- D4 - Bi-Color Green/Yellow Led used for User Led 2/Link/Activity

- D5 – Bi-Color Red/Green Led used to determine VADJ
  - If Green – VADJ = 1.8V
  - If Red -- VADJ = 2.5V
  - If Orange – VADJ = 3.3V
- D6 – Yellow Led used to determine if Power Good is present
- D7 - Bi-Color Red/Green Led used for 8kHz PTP sync status User LED

### 3.8 Ethernet PHY Clock source - 25MHz x 2

The Ethernet PHY clock is a 25 MHz Microchip clock DSC1121DI2-025.0000 demonstrated to work with the Microchip PHY. This clock has a 25 PPM in order to meet the PHYs minimum 25MHz clock requirements. Each clock source has 49.9 Ohm termination resistors on their source

### 3.9 Ethernet MAC FMC Clock source - 125MHz x 1

The MAC FMC clock will be a 125 MHz Microchip clock DSC1123CI2-125.0000.

## 4 Mechanical Requirements

The following figures illustrate the I/O connector area on an FMC module.

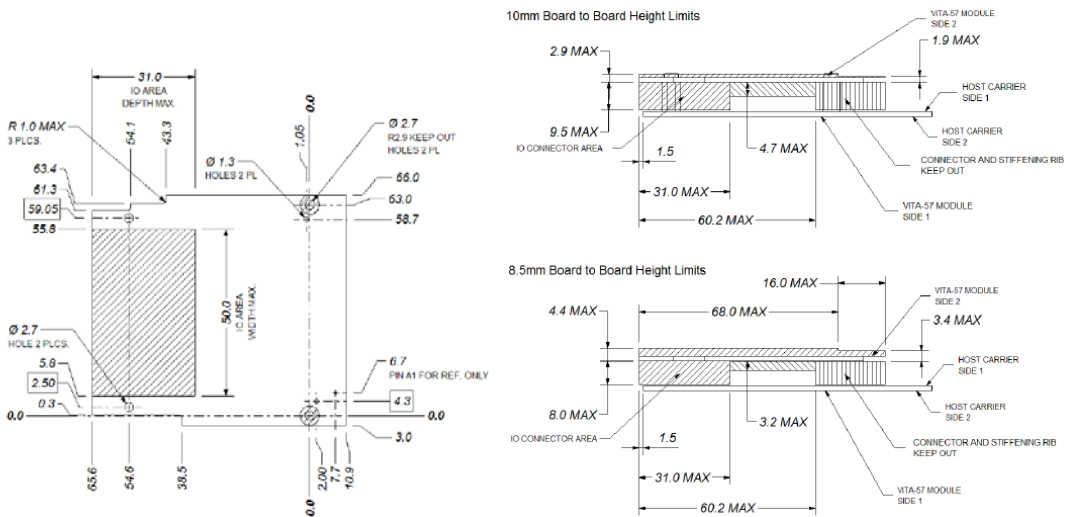


Figure 4 -- I/O Connector Area

## 5 Disclaimer

Avnet assumes no liability for modifications that the owner chooses to make to their Network FMC board.